AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all previous versions, and listings, of claims in the present application.

Please cancel claims 1 and 11-17 without prejudice or disclaimer.

1. (Canceled).

2. (Currently amended) ~~The EEPROM as claimed in claim 1,~~ An EEPROM having a memory transistor, said memory transistor comprising:

a drain region of a second conductivity type formed in a superficial layer of a semiconductor substrate of a first conductivity type, said drain region including an embedded layer and a drain side field moderating layer formed adjacent to said embedded layer;

a source region of the second conductivity type in the superficial layer of said semiconductor substrate;

a channel region between said drain region and said source region;

a gate insulating film formed on a surface of said semiconductor substrate;

a tunnel film formed in a part of said gate insulating film above said embedded layer;

a floating gate electrode formed above said tunnel film and said channel region and having a shape such that it has a size enough to cover said tunnel film and has a gate length approximately equal to a length of said channel region between said drain region and said source region;

an interlayer insulating film covering an upper face and side faces of said floating gate electrode; and

a control gate electrode formed above said floating gate electrode interposing said interlayer insulating film therebetween,

wherein said control gate electrode is shaped to be wider than said floating gate electrode and to wrap said floating gate electrode above said tunnel film and is shaped to be narrower than said floating gate electrode above said channel region.

3. (Currently amended) ~~The EEPROM as claimed in claim 1,~~ An EEPROM having a memory transistor, said memory transistor comprising:

a drain region of a second conductivity type formed in a superficial layer of a semiconductor substrate of a first conductivity type, said drain region including an embedded layer and a drain side field moderating layer formed adjacent to said embedded layer;

a source region of the second conductivity type in the superficial layer of said semiconductor substrate;

a channel region between said drain region and said source region;

a gate insulating film formed on a surface of said semiconductor substrate;

a tunnel film formed in a part of said gate insulating film above said embedded layer;

a floating gate electrode formed above said tunnel film and said channel region and having a shape such that it has a size enough to cover said tunnel film and has a gate length approximately equal to a length of said channel region between said drain region and said source region;

an interlayer insulating film covering an upper face and side faces of said floating gate electrode; and

a control gate electrode formed above said floating gate electrode interposing said interlayer insulating film therebetween

wherein said floating gate electrode and said control gate electrode each have an opening and the position of the opening in the control gate electrode offsets toward said channel region so that said control gate electrode wraps said floating gate electrode above said tunnel film and is narrower than said floating gate electrode above said channel region.

4. (Original) An EEPROM of a floating gate type and a two-layer polysilicon type having a memory transistor and a select transistor for selecting said memory transistor, said memory transistor comprising:

an embedded layer of a second conductivity type formed in a superficial layer of a semiconductor substrate of a first conductivity type;

a drain side field moderating layer of the second conductivity type formed adjacent to said embedded layer in the superficial layer of said semiconductor substrate;

a source region of the second conductivity type in the superficial layer of said semiconductor substrate;

a channel region between said drain side field moderating layer and said source region;

a gate insulating film formed on a surface of said semiconductor substrate;

a tunnel film formed in a part of said gate insulating film above said embedded layer;

a floating gate electrode formed above said tunnel film and said channel region and having a shape such that it entirely covers said tunnel film and covers neither said source region nor said drain side field moderating layer;

an interlayer insulating film covering an upper face and side faces of said floating gate electrode; and

a control gate electrode formed above said floating gate electrode interposing said interlayer insulating film therebetween,

wherein said source region and said drain side field moderating layer are self-alignigly formed by ion implantation using said floating gate electrode as a mask, and

wherein said control gate electrode is shaped to be wider than said floating gate electrode and to wrap said floating gate electrode above said tunnel film and is shaped to be narrower than said floating gate electrode above said channel region.

5. (Original) The EEPROM as claimed in claim 4, wherein said select transistor has a gate electrode and a source region, the EEPROM further comprising a source side field moderating layer of the second conductivity type in at least one of source regions of said memory transistor and said select transistor, said source side field moderating layer being self-alignigly formed by ion implantation using said floating gate electrode or said gate electrode as a mask.

6. (Original) The EEPROM as claimed in claim 5, further comprising a source layer of the second conductivity type offset against said source side field moderating layer and having a higher concentration than said source side field moderating layer, so that at least one of said memory transistor and said select transistor has an offset type source structure.

7. (Original) The EEPROM as claimed in claim 4, wherein said select transistor has a gate electrode formed simultaneously with said floating gate electrode of said memory transistor from a first polysilicon layer.

8. (Original) The EEPROM as claimed in claim 4, wherein said select transistor has a drain side field moderating layer in a drain region, said drain side field moderating layer being formed simultaneously with said drain side field moderating layer of said memory transistor and self-aligningly by ion implantation using said gate electrode as a mask.

9. (Original) The EEPROM as claimed in claim 4, wherein said interlayer insulating film includes a nitride film and is formed on said semiconductor substrate including a surface of said gate electrode in a whole region of said select transistor and said memory transistor.

10. (Original) The EEPROM as claimed in claim 4, further comprising an insulation film for element separation formed on the surface of said semiconductor substrate, wherein a length of a region where said tunnel film is formed is regulated by said insulation film.

Claims 11-17 (Canceled).